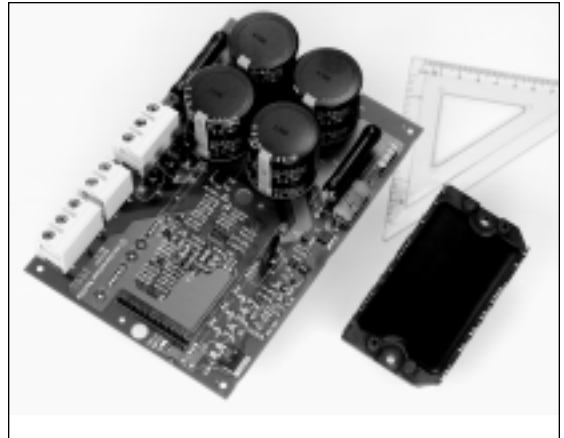


## Integrated Power Stage for 3 hp Motor Drives

- 3 hp (2.2 kW) power output  
Industrial rating at 150% overload for 1 minute
- 380 - 480V AC input, 50/60Hz
- Available as complete system or sub-system assemblies

### Power Module

- 3-phase rectifier bridge
- 3-phase, short circuit rated, ultrafast IGBT inverter
- Brake IGBT and diode
- Low inductance (current sense) shunts in positive and negative DC rail
- NTC temperature sensor
- Pin-to-base plate isolation 2500V rms
- Easy-to-mount two-screw package
- Case temperature range -25°C to 125°C operational



### Driver-Plus Board

- DC bus capacitor filter with NTC inrush current limiter
- IR2233 monolithic 3-phase HVIC driver
- Driver stage for brake transistor
- On-board +15V and +5V power supply
- MOV surge suppression at input
- DC bus voltage and current feedback
- Protection for short-circuit, earth/ground fault, overtemperature and overvoltage
- Terminal blocks for 3-phase input/output and brake connections

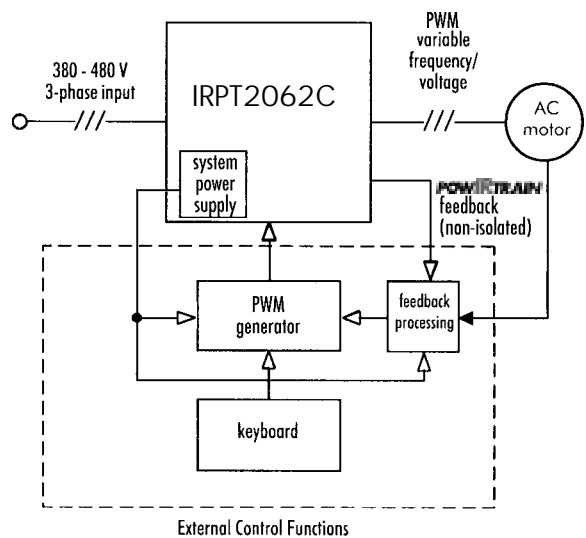


Figure 1. The IRPT2062 **POWIRTRAIN** within a motor control system

## System Description

The IRPT2062C **POWERTRAIN** provides the complete power conversion function for a 3hp (2.2kW) variable-frequency, variable-voltage, AC motor controller. The **POWERTRAIN** combines a power assembly IRPT2051A with a Driver-Plus Board IRPT2051D. Figure 1 shows the block diagram of the **POWERTRAIN** within an AC motor control system.

The power module contains a 3-phase input bridge rectifier, 3-phase IGBT and diode, 3-phase IGBT inverter, current sense shunts, and a thermistor. It is designed for each mounting to a heat sink.

The Driver-Plus Board contains DC link capacitors, capacitor soft charge function using NTC thermistor, surge suppression MOVs, IGBT gate drivers, DC bus voltage and current feedback signals, protection circuitry and local power supply. It is designed to mate with a controller board through a single row header. Terminal blocks are also provided on the Driver-Plus Board for all end-user line input, motor output, and brake resistor.

Output power is Pulse-Width Modulated (PWM), 3-phase, variable-frequency, variable voltage controlled by an externally-generated user-provided PWM controller for inverter IGBT switching. The power supply offers the user non-isolated 5V and 15V to power the microcontroller.

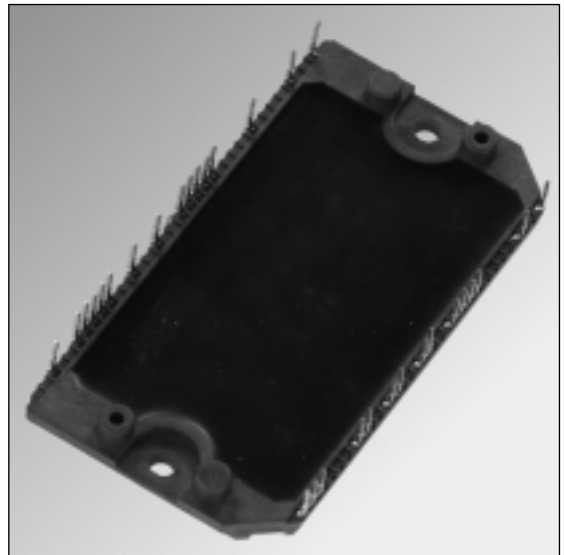
The IRPT2062C offers several benefits to the drive manufacturer as listed below:

- It eliminates component selection, design layout, interconnection, gate drive, local power supply, thermal sensing, current sensing, and protection.
- Gate drive and protection circuits are designed to closely match the operating characteristics of the power semiconductors. This allows power losses to be minimized and power rating to be maximized to a greater extent than is possible by designing with individual components.
- It reduces the effort of calculating and evaluating power semiconductor losses and junction temperature.
- It reduces the manufacturer's part inventory and simplifies assembly.

[**POWERTRAIN** specifications and ratings are given for system input and output voltage and current, power losses and heat sink requirements over a range of operating conditions. **POWERTRAIN** system ratings are verified by IR in final testing.]

## The IRPT2062A Power Module

The IRPT2062A power module, shown in figure 2, is a chip and wire epoxy-encapsulated module. It houses input rectifiers, brake IGBT and freewheeling diode, output inverter, current sense shunts and NTC thermistor. The 3-phase **input bridge rectifiers** are rated at 1600V. The brake circuit uses 1200V IGBT and free-wheeling diode. The inverter section employs 1200V, **short circuit rated, ultrafast IGBTs** and **ultrafast freewheeling diodes**. Current sensing is achieved through **25 mΩ low-inductance shunts** provided in the positive and negative DC bus rail. The **NTC thermistor** provides temperature sensing capability. The lead spacing on the power module meets UL840 pollution level 3 requirements.



**Figure 2.** IRPT2062A Power Module

The power circuit and layout within the module are carefully designed to minimize inductance in the power path, to reduce noise during inverter operation and to improve the inverter efficiency. The Driver-Plus Board required to run the inverter can be soldered to the power module pins, thus minimizing assembly and alignment. The power module is designed to be mounted to a heat sink with two screw mount positions, in order to insure good thermal contact between the module substrate and the heat sink.

## The IRPT2062D Driver-Plus Board

The Driver-Plus Board, shown in figure 3, is the interface between the controller and the power stage. It contains the IGBT gate drivers, protection circuitry, feedback, brake drive and local power supply. The driver also interfaces to the AC input line. It houses the DC link capacitors, NTC in-rush limiting thermistor, and surge suppression MOVs.

The inverter **gate drive circuits**, implemented with an IR2233 monolithic 3-phase HVIC driver, delivers gate drive to the IGBTs corresponding to PWM control signals  $\overline{IN1}$  through  $\overline{IN6}$ . It introduces a 0.2  $\mu\text{s}$  dead time between upper and lower gate signals for each phase. Any additional dead time necessary must be included in the PWM signals. After a fault condition all inverter gate drivers are disabled and latched. The  $\overline{FAULT}$  pin is also pulled low through an open drain which illuminates a red LED. Gate drives must be enabled with an active low pulse

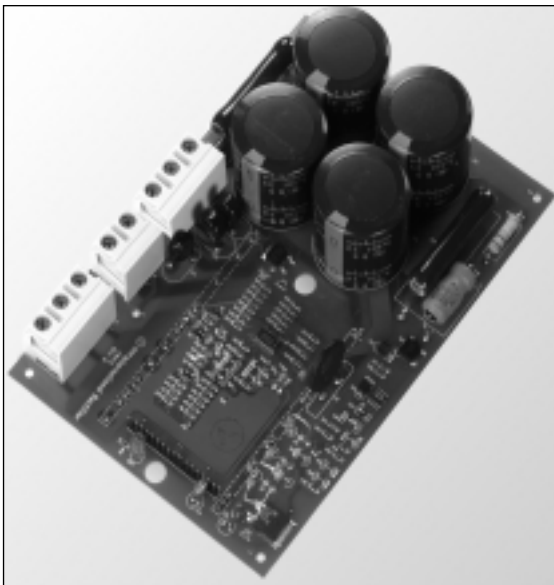


Figure 3. IRPT2062D Driver-Plus Board

applied to the  $\overline{RESET}$  pin while PWM inputs  $\overline{IN1}, \dots, \overline{IN6}$  are held high (off condition). The  $\overline{FAULT}$  condition can also be set by the controller through an active high signal on the STOP pin. After power-up, the  $\overline{RESET}$  pin must be pulled low before any input signals are activated.

The **protection circuitry** will set a  $\overline{FAULT}$  for short-circuit, earth-fault, over-temperature, or over-voltage conditions as specified. Current signals are sensed through shunts in positive and negative DC bus rails. Earth faults are sensed using the high-side shunt and the signal is fed through an opto-isolator to the protection circuitry. Over-voltage is sensed through a resistor divider from the positive DC bus. Over-temperature protection is obtained using a thermistor inside the power module. A  $\overline{FAULT}$  condition occurs if the temperature of the power module's IMS substrate exceeds the trip level. The system is designed for 150% overload for one minute while operating with the specified heat sinks. The controller should shut off the PWM signals if the overload persists for more than one minute.

The **feedback signals** used by the protection circuitry are also available to the controller. The current feedback signal from the low-side shunt is available on the IFB pin at 0.025 V/A. If filtering of this signal is required, it should be done by adding a high-impedance buffer stage between signal and filter. The DC bus reference is provided on VFB. This reference has been scaled down by a factor of 100 and should also be protected with a high-impedance buffer stage.

The **brake function** is implemented by connecting a power resistor between the terminals on the Brake terminal block. The value and power of the resistor determines maximum braking capability along with the rating of the brake IGBT. The input signal on IN7 is active low and CMOS or LSTTL compatible.

The **switching power supply** employs an IR2152 self-oscillating driver chip in a buck regulator topology to deliver a nominal 15V and 5V DC with respect to the negative bus (N). The power supply feeds the gate drive and protection circuits. The 15V ( $V_{CC}$ ) and 5V ( $V_{DD}$ ) outputs are available on the control interface for powering the user's control logic.

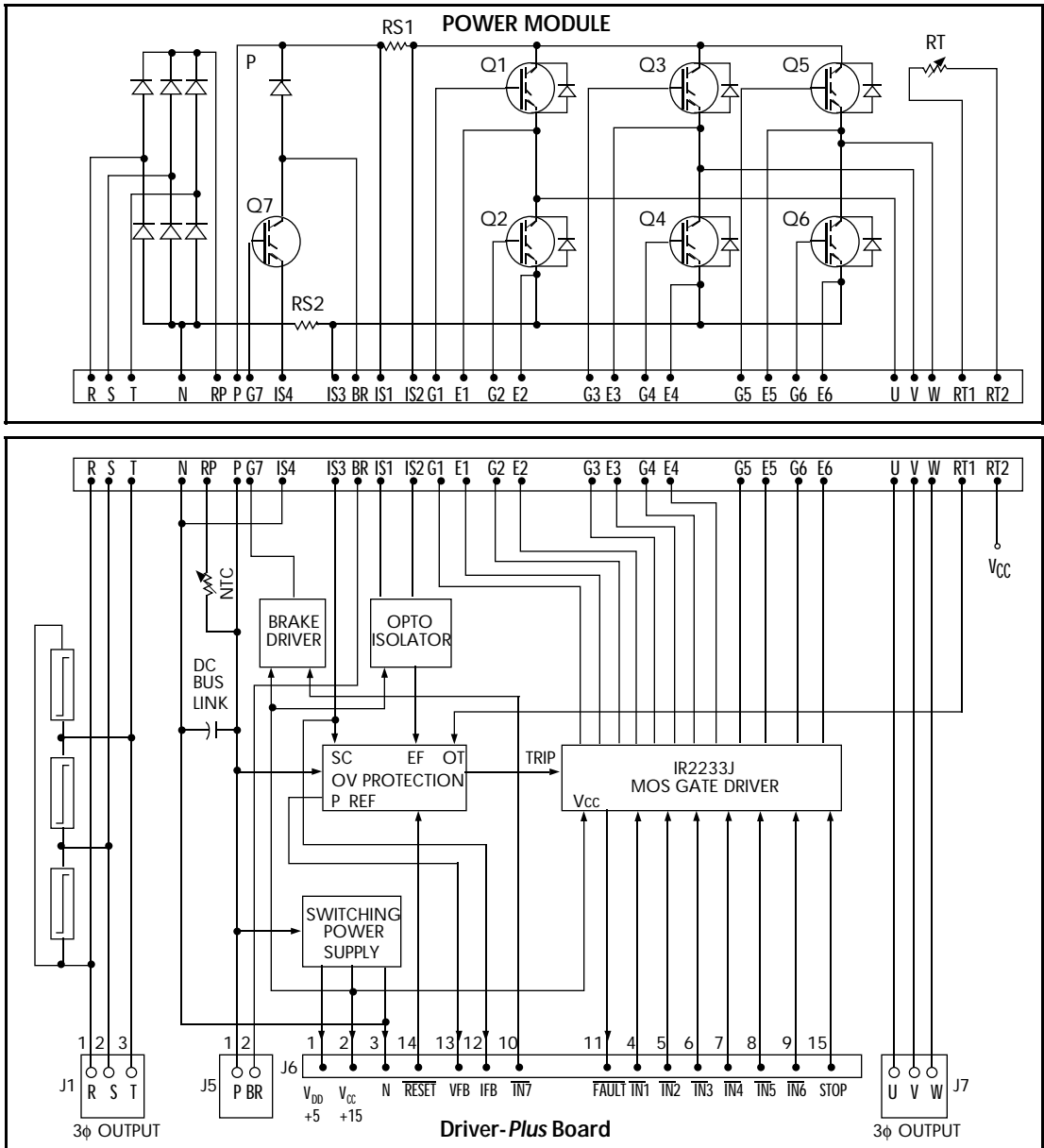
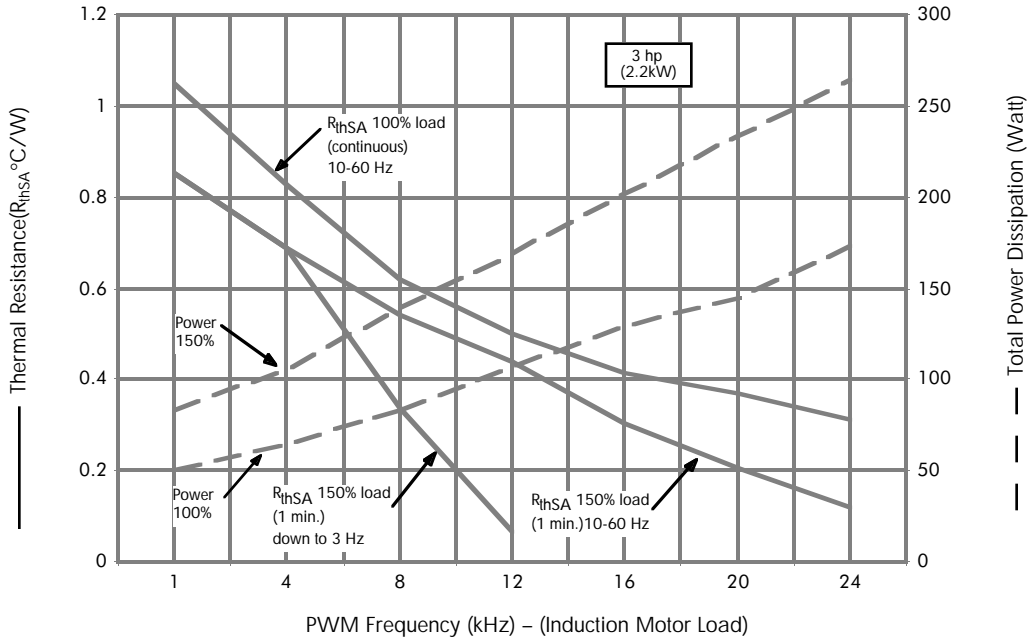


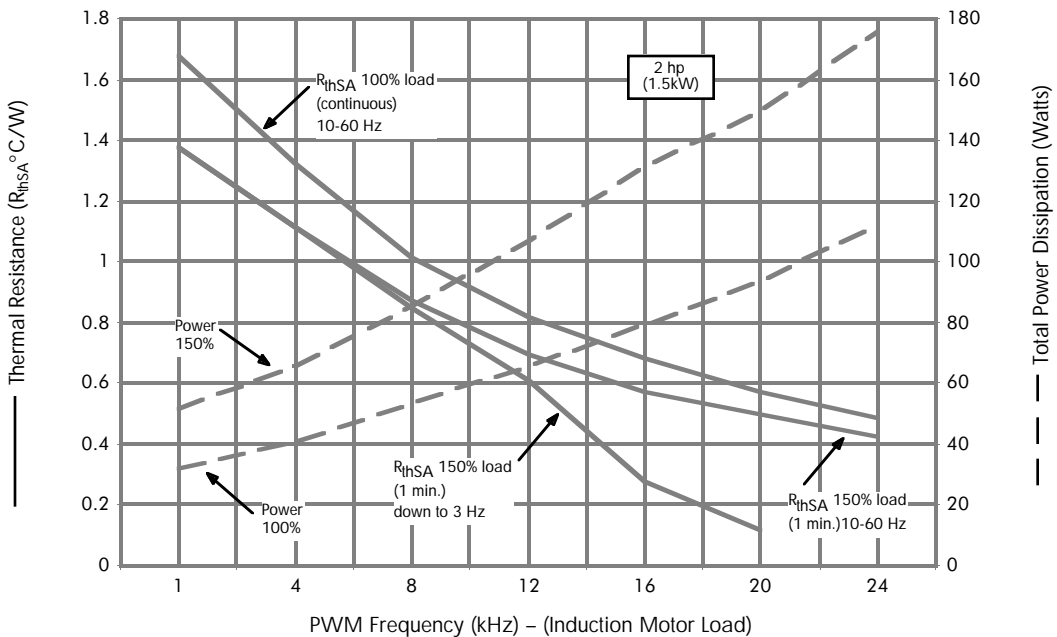
Figure 4. IRPT2062C Basic Architecture

Specifications

PARAMETERS	VALUES	CONDITIONS
<i>Input Power</i>		
Voltage	380V, -15%, 480V +10%	
Frequency	50/60 Hz	
Input current	8.26A rms @ nominal output 125 A peak	$T_A = 40^\circ\text{C}$ , $R_{thSA} = 0.69^\circ\text{C}/\text{W}$ Initial bus capacitor charging
<i>Output Power</i>		
Voltage	0 - 480V rms	defined by external PWM control
Nominal motor hp (kW)	3hp (2.2 kW) nominal full load power 150% overload for 1 minute	$R_{thSA} = 0.69^\circ\text{C}/\text{W}$ , $V_{in} = 460\text{V AC}$ , $f_{PWM} = 4\text{kHz}$ , $f_o = 60\text{ Hz}$ , $T_A = 40^\circ\text{C}$ , $Z_{thSA}$ limits $\Delta T_C$ to $10^\circ\text{C}$ during overload
Nominal motor current	5.90A rms nominal full load current 8.85A rms 150% overload for 1 minute	
<i>Control Inputs</i>		
IN1...IN6, (PWM), IN7 (Brake), RESET	5V maximum, active low	CMOS, LSTTL compatible, open collector
STOP	5V maximum, active high	CMOS or LSTTL compatible
Pulse deadtime	0.2 $\mu\text{sec}$ typical, set by IR2233	maximum set by controller
Minimum input pulse width	1.0 $\mu\text{sec}$	
<i>Protection</i>		
Output current trip level	28A peak, $\pm 10\%$	$T_C = 25^\circ\text{C}$
Earth fault current trip level	50A, $\pm 10\%$	$T_C = 25^\circ\text{C}$
Overtemperature trip level	100°C, $\pm 5\%$	Case temperature
Overvoltage trip level	850V, $\pm 10\%$	
Maximum DC link voltage	760V	user to ensure rating not exceeded >30 sec
Short circuit shutdown time	2.5 $\mu\text{sec}$ typical	output terminals shorted
<i>Feedback Signals</i>		
Current feedback (IFB)	0.025V/A <sub>BUS</sub> typical	$T_C = 25^\circ\text{C}$
DC bus voltage feedback (VFB)	0.010V/V <sub>BUS</sub> typical	$T_C = 25^\circ\text{C}$
Fault feedback (FAULT)	5V maximum, active low	CMOS or LSTTL compatible
<i>On Board Power Supply</i>		
V <sub>CC</sub>	15V, $\pm 10\%$	
V <sub>DD</sub>	5V, $\pm 5\%$	
I <sub>CC</sub> + I <sub>DD</sub>	60 mA	available to user
<i>Brake</i>		
Current	10.5A	
<i>Module</i>		
Isolation voltage	2500V rms	pin-to-baseplate isolation, 60 Hz, 1 minute
Operating case temperature	-25°C to 125°C	95% RH max. (non-condensing)
Mounting torque	1 N·m	M4 screw type
<i>System Environment</i>		
Ambient operating temp. range	0 to 40°C	95% RH max. (non-condensing)
Storage temperature range	-25 to 60°C	



**Figure 5a.** 3 hp/5.9A Output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency



**Figure 5b.** 2 hp/4.2A Output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency

NOTE: For Figures 5a and 5b: Operating Conditions:  $V_{in} = 460V_{rms}$  MI = 1.15, PF = 0.8,  $T_A = 40^{\circ}C$ ,  $T_J < 145^{\circ}C$ ,  $T_S < 95^{\circ}C$ ,  $Z_{thSA}$  limits  $\Delta T_C$  during 1 minute overload to  $10^{\circ}C$

# Mounting, Hookup and Application Instructions

## Mounting

1. Remove all particles and grit from the heat sink and power substrate.
2. Spread a .004" to .005" layer of silicone grease on the heat sink, covering the entire area that the power substrate will occupy. Recommended heat sink flatness is .001 inch/inch and Total Indicator Readout (TIR) of .003" below substrate.
3. Place the power substrate onto the heat sink with the mounting holes aligned and press it firmly into the silicone grease.
4. Place the 2 M4 mounting screws through the PCB and power module and into the heat sink and tighten the screws to 1 Nm torque.

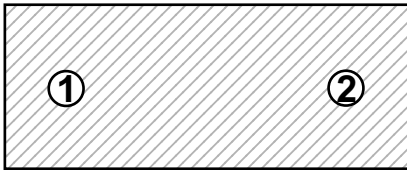


Figure 6. Power Module Mounting Screw Sequence

## Control Connections

All input and output connections are made via a 16-terminal female connector to J6.

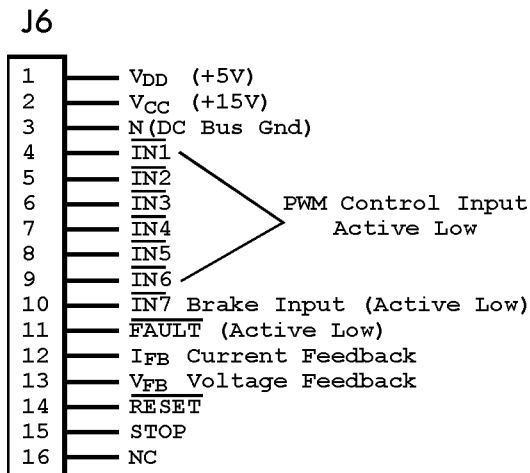


Figure 7a. Control Signal Connector

## Power Connections

3-phase input connections are made to terminals R, S and T (J1). Inverter output terminal connections are made to terminals U, V and W (J7).

Positive DC bus and Brake IGBT collector connections are brought out to terminals P (positive) and BR (brake) of J5 connector. An external resistor for braking can be connected across these terminals.

## Power-Up Procedure

When 3-phase input power is first switched on, PWM inputs to the IRPT2062 must be inhibited (held high) until the protection latch circuitry is reset. To reset this latch before inverter start-up, RESET pin on J6 connector must be pulled down low for at least 2  $\mu$ sec. This will set the FAULT feedback signal high. Now, the PWM input signals can be applied for inverter start-up.

## Power-Down Procedure

The following sequence is recommended for normal power down:

1. reduce motor speed by PWM control
2. inhibit PWM inputs
3. disconnect main power.

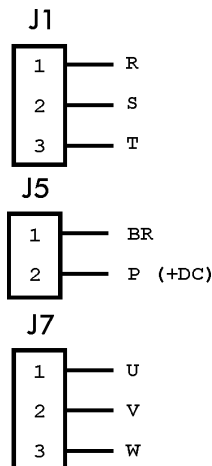
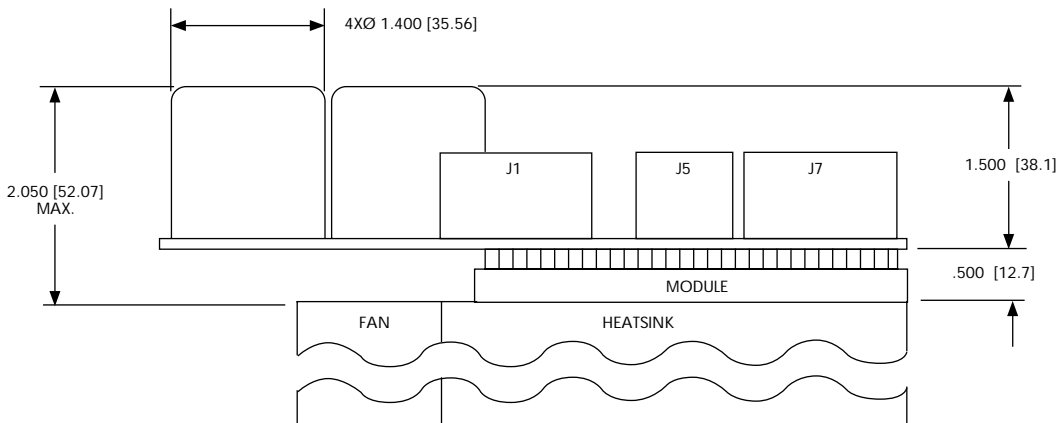
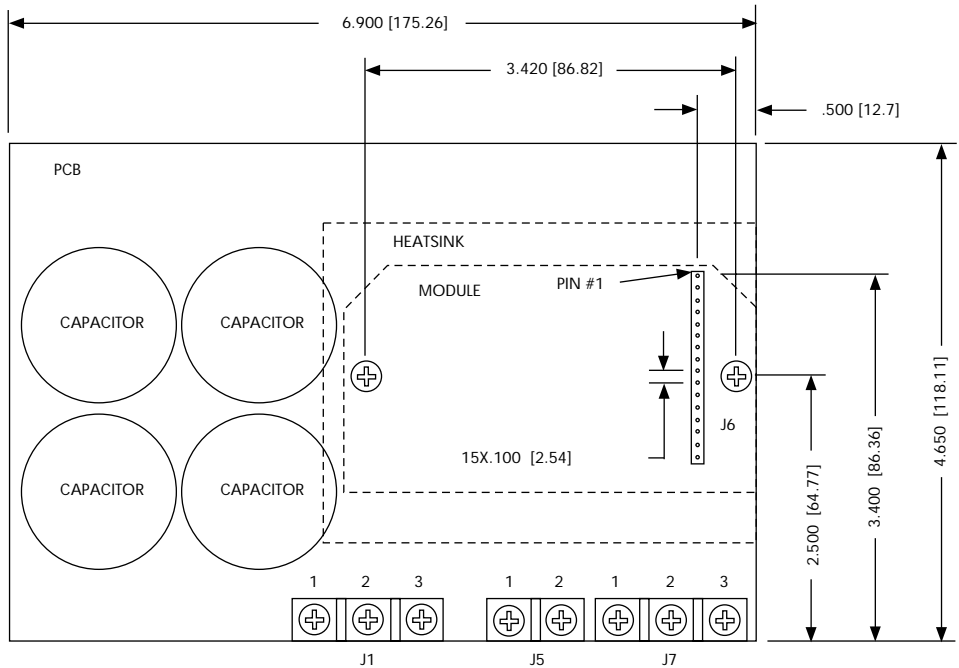


Figure 7b. Input and Output Terminal Blocks

## IRPT2062D Mechanical Specifications

NOTE: Dimensions are in inches (millimeters)







## Part Number Identification and Ordering Instructions

### IRPT2062A Power Assembly

Chip and wire epoxy encapsulated module with 1600V input rectifiers, 1200V brake IGBT and freewheeling diode, 1200V short-circuit rated, ultra-fast IGBT inverter with ultra-fast freewheeling diodes, temperatures sensing NTC thermistor and current sensing low-inductance shunts.

### IRPT2062C Complete **POWERTRAIN**

IRPT2062A Power Module and IRPT2062D Driver-Plus Board pre-assembled and tested to meet all system specifications.

### IRPT2062D Driver-Plus Board

Printed circuit board assembled with DC link capacitors, NTC in-rush limiting thermistor, high-power terminal blocks, surge suppression MOVs, IGBT gate drivers, protection circuitry and low power supply. The PCB is functionally tested with standard power module to meet all system specifications.

### IRPT2062E Design Kit

Complete **POWERTRAIN** (IRPT2062C) with full set of design documentation including schematic diagram, bill of material, mechanical layout, schematic file, Gerber files and design tips.

## Functional Information

**CAUTION:** All control logic is referenced to the negative power bus, which is live with respect to earth/ground.

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### *Capacitor Soft Charge*

A dc bus capacitor is connected to the rectifier bridge output through an NTC. At power-up, the NTC limits the maximum inrush current to the rated peak input current, though normal line impedance will impact the inrush insignificantly. During normal operation, current through the NTC reduces its resistance, hence reducing its losses. In the event of a brief power loss, the NTC will not limit the recharge of the bus because its temperature will not have time to reduce back to ambient.

### *System Power Supply*

A buck converter designed with the IR2152 self-oscillating half-bridge driver generates  $V_{CC}$  (15V) and  $V_D$  (5V) for drive and protection circuits. It draws its power from the midpoint of the dc bus, which is regulated to half of the voltage. Both  $V_{CC}$  and  $V_D$  are available at the control connector through microprocessor controls. Rated output current is the sum of  $I_{CC}$  and  $I_D$ .

Floating power supplies for high side devices are derived through the bootstrap technique, simplifying power supply requirements.

### *Gate Drive Circuits*

Gate drive for the inverter is implemented with an IR2233 monolithic 3-phase HVIC driver. An under voltage circuit monitors the local power supply voltage. It will set the FAULT and inhibit the PWM output in the event of a low power condition to protect the IGBTs from excessive power loss due to low gate drive.

A short circuit buffer power supply counters the voltage drop across the shunt in the negative dc bus, allowing the device to have nominal gate voltage during short circuit. This will maintain the current to a detectable level.

The brake IGBT is generally switched at low frequency, so a simple bipolar gate drive circuit is used to drive it.

### *System Protections*

**Short circuit** is monitored through a shunt in the negative bus, which detects phase-to-phase and phase-to-earth short circuits (when current flows from earth to negative bus). The voltage drop across the shunt is compared to a pre-set limit and when the current exceeds the rated nominal value, this protection is activated. The shunt signal is available to the user on the control interface as  $I_{FB}$ . Since this is the same node that is used by this protection circuit, any external connection should be done through a high impedance buffer stage.

**Earth/ground fault** from positive bus to earth is detected through the shunt in the positive bus and an opto-coupler. When fault current exceeds the rated nominal value, this protection is activated.

**Over temperature** is measured by a thermistor mounted close to the inverter section in the power module. When the substrate temperature exceeds the nominal rated temperature, this protection is activated.

**Over voltage** is detected by comparing attenuated dc bus voltage with a pre-set reference. When the bus voltage exceeds the nominal rated value, this protection is activated. The attenuated dc bus voltage is available to the user on the control interface as  $V_{FB}$ . Since this is the same node that is compared to the reference, any external connections should be done through a high impedance buffer stage.

If any of the protection features are activated, the TRIP signal goes high activating the internal latch of the IR2233. This turns off all gate outputs to the inverter and acknowledges the FAULT to the controller.

### *Trip Reset*

The FAULT signal can be removed by pulling down the RESET pin for 2  $\mu$ s. This should be done only after all inputs, IN1...IN6, are inactive. The system protections cannot be disabled by tying this pin to N because the fault logic takes precedence over the reset.

## Interface With System Controller

All signals are referred to the negative dc bus (N).  $\overline{IN1}... \overline{IN7}$  are TTL/CMOS compatible active low signals. Maximum voltage rating for these signals is 5V. All channels are provided with pull-up resistors and can be used with open collector inputs.

$\overline{FAULT}$  is an open drain, active low signal, provided with a pull-up and a red LED. Typical current sink capacity for this pin is 5 mA. This pin should not be directly connected to an npn transistor base as it would appear to always be in  $\overline{FAULT}$  mode.

$V_{FB}$  and  $I_{FB}$  are the scaled down dc bus voltage and bus current respectively. The on-board protection circuitry use these signals for sensing fault conditions. Any connection to these signals should be done through a high impedance buffer stage as not to disrupt the protection circuits.

## Heat Sink Requirements

Figures 5a and 5b (page 6) show the thermal resistance of the heat sink required for various output power levels and PWM switching frequencies. Maximum total losses of the unit are also shown.

This data assumes the following key operating conditions:

- The maximum continuous combined losses of the rectifier and inverter occur at full pulse with modulation. These

losses set the maximum continuous operating temperature of the heat sink.

- The maximum combined losses of the rectifier and inverter at full PWM under overload set the incremental temperature rise of the heat sink during overload, which is limited to 10°C due to  $Z_{THSA}$ .
- The minimum output frequency at which full overload current is to be delivered sets the peak IGB junction temperatures.
- At low output frequency IGBT junction temperatures tends to follow the instantaneous fluctuations of the output current. Thus, peak junction temperature rise increases as output frequency decreases.

## Voltage Rise During Braking

The motor will feed energy back to the DC link during electric braking, forcing DC bus voltage to rise above the level defined by input line voltage. Deceleration of the motor must be controlled by appropriate PWM control to keep the DC bus voltage within the rated maximum value. For high inertial loads, or for very fast deceleration rates, this can be achieved by the brake provided in the system by connecting an external braking resistor between terminals P and BR.  $\overline{IN7}$  controls the brake transistor switching.